ABSTRACT OF THE DISCLOSURE

The semiconductor device comprises a semiconductor substrate 14 of a first conduction type; a buried semiconductor layer 38b of a second conduction type formed in a first region of the semiconductor substrate 14, spaced from a surface of the semiconductor substrate 14; a semiconductor region 38a of a second conduction type formed in a peripheral portion of a region between the surface of the semiconductor substrate 14 in the first region of the semiconductor substrate 14 and the buried semiconductor layer 38b, and connected to the buried semiconductor layer 38b; and a semiconductor region 14a of the first conduction type formed in the semiconductor substrate 14 surrounded by the buried semiconductor layer 38b and the second conduction type semiconductor region 38a. The parasitic capacitance between the source/drain diffused layer of the input/output transistor and the semiconductor substrate can be small, whereby the semiconductor device can have high operational speed. The leak current from the capacitor through the junction between the source/drain diffused layer of the transistor of the cell unit and the first conduction type semiconductor region can be small, with a result that frequent rewriting operations for retaining a charge of the capacitor are not necessary, and the semiconductor device can have small electric power consumption.